The following listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A varactor structure comprising:

a semiconductor substrate of a first conductivity type, said substrate including a subcollector of a second conductivity type located below an upper region of said substrate, said first conductivity type is different from said second conductivity type;

a well region located in said upper region of said substrate, wherein said well region includes outer well regions of said second conductivity type and an inner well region of said first conductivity type, each well of said well region is separated at an upper surface by an isolation region and each outer well region has an upper surface which includes a source/drain region; and

a field effect transistor having at least a gate conductor of said first conductivity type located above said inner well region.

Claim 2 (Original) The varactor structure of Claim 1 wherein said first conductivity type comprises a p-type dopant and second conductivity type comprises a n-type dopant.

Claim 3 (Original) The varactor structure of Claim 1 wherein said first conductivity type comprises a n-type dopant and said second conductivity type comprises a p-type dopant.

Claim 4 (Cancelled)

Claim 5 (Original) The varactor structure of Claim 1 wherein each well region extends beneath the isolation region such that neighboring well regions are in contact with each other.

Claim 6 (Original) The varactor structure of Claim 1 wherein said upper region of said substrate comprises an epitaxial semiconductor layer.

Claim 7 (Original) The varactor structure of Claim 1 wherein said field effect transistor further comprises a gate dielectric located beneath said gate conductor, a hard mask located on said gate conductor, at least one spacer located on sidewalls of said gate conductor and abutting source/drain regions.

Claim 8 (Original) The varactor structure of Claim 1 wherein said gate conductor comprises polysilicon.

Claim 9 (Currently Amended) A varactor structure comprising

a p-type semiconductor substrate, said p-type substrate including an n-type subcollector located below an upper region of said substrate;

a well region located in said upper region of said substrate, wherein said well region includes outer N-well regions and an inner P-well region, each well of said well region is separated at an upper surface by an isolation region and each outer well region has an upper surface which includes a source/drain region; and

a field effect transistor having at least a p-type gate conductor located above said inner P-well region.

Claim 10 (Cancelled)

Claim 11 (Original) The varactor structure of Claim 9 wherein each well region extends beneath the isolation region such that neighboring well regions are in contact with each other.

Claim 12 (Original) The varactor structure of Claim 9 wherein said upper region of said substrate comprises an epitaxial semiconductor layer.

Claim 13 (Original) The varactor structure of Claim 9 wherein said field effect transistor further comprises a gate dielectric located beneath said gate conductor, a hard mask located on said gate conductor, at least one spacer located on sidewalls of said gate conductor and abutting source/drain regions.

Claim 14 (Original) The varactor structure of Claim 9 wherein said gate conductor comprises polysilicon.

Claim 15 (Withdrawn) A method of fabricating a varactor structure comprising the steps of:

providing a structure that comprises a semiconductor substrate of a first conductivity type;

forming a plurality of isolation regions in said upper region of said substrate;

forming a well region in said upper region of said substrate, wherein said well region includes outer well regions of a second conductivity type that differs from said first conductivity type and an inner well region of said first conductivity type, each well of said well region is separated at an upper surface by an isolation region; and

forming a field effect transistor having at least a gate conductor of said first conductivity type above said inner well region, wherein a doped region of the second conductivity type is formed into an upper region of said substrate prior to, or immediately after forming said plurality of isolation regions.

Claim 16 (Withdrawn) The method of Claim 15 wherein said first conductivity type comprises a p-type dopant and second conductivity type comprises an n-type dopant.

Claim 17 (Withdrawn) The method of Claim 15 wherein said first conductivity type comprises a n-type dopant and said second conductivity type comprises a p-type dopant.

Claim 18 (Withdrawn) The method of Claim 15 wherein said doped region comprises a subcollector or an isolation well that is formed by ion implantation.

Claim 19 (Withdrawn) The method of Claim 15 wherein said upper region of said substrate comprises an epitaxial grown semiconductor layer which is formed after forming the doped region.

Claim 20 (Withdrawn) The method of Claim 15 wherein forming said well region comprises masked ion implantation processes.